PATENT

Docket No.: ACT-307DVA

#13 Aff. Dec. M. Brunson 6/4/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2814 Examiner: Mai, Anh D.

Serial No. 10/036,303 Filed: December 28, 2001

In Re Application of: Frank Hawley

For: METHOD FOR FABRICATING A MOS TRANSISTOR HAVING IMPROVED TOTAL REDIATION-INDUCED LEAKAGE CURRENT

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to ~~Director of Patents, Box Amendment, Washington, D.C. 20231~~ on 5/27/03 *Signed* [signature]

MS Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

DECLARATION UNDER 37 CFR 1.132

I, Frank Hawley, declare and state as follows:

1. I have been employed by Actel Corporation, the assignee of the invention disclosed and claimed in the above-identified patent application, for 12 years.

2. I received a Bachelor of Science degree in Electrical Engineering from Clarkson University in 1979.

3. I have been continuously engaged in electronic design since 1980.

4. As result of my education and experience, I believe myself to be one of ordinary skill in the art of transistor design and radiation tolerance.

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5. I have reviewed the specification as originally drafted. I have reviewed the amendments to the specification stating at page 8 lines 14-15 that "MOS transistor 50 is formed in silicon substrate 52 between two shallow portions shown in FIG. 3 of an annular trench isolation structure filled with deposited silicon dioxide 54 as in the prior art shallow-trench isolated transistor FIG. 2." A person of ordinary skill in the art would immediately understand that an isolation trench, by definition, isolates or, in other words, completely surrounds a device such as a transistor. An isolated active area must be surrounded by a single isolation trench. Thus, a cross-sectional view of an annular trench would necessarily show two portions of one annular trench isolation structure. The Examiner is mistaken when he states that a "portion of the specification indicates that the active area is surrounded not by one but by two trench isolation structures".

5. I have reviewed the amendments to the specification and the amendments to the claims. The amended specification correctly states the design of the transistor and the trench surrounding and isolating the transistor. I have also reviewed the amended claims which, as amended, properly state the design of the transistor and the annular trench surrounding the transistor.

5. As in my previous declaration, I have examined Figures 3 and 4a through 4c of the above-identified patent application and I conclude that any person of

ordinary skill in the art, examining this figure, would recognize that Figures 3 and 4a through 4c clearly show a view of a cross section of an annular transistor having a single isolation trench. Because this is a cross-sectional view, it shows one isolation trench that surrounds one (or more) transistor. Therefore, the fact that this is a cross-sectional view of an annular transistor means that the fact that this is a single isolation trench is inherently disclosed in the application.

A single trench can and does describes a trench that surrounds one or more transistors. The trench can be seen as a moat surrounding a body of land. Thus, a single trench can and does define an annular transistor having a single isolation trench as inherently disclosed in the present application.

I, the undersigned, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Frank Hawley

May 14, 2003